



(19)

(11) Publication number: 10209347

Generated Document.

## PATENT ABSTRACTS OF JAPAN

(21) Application number: 09367985

(51) Intl. Cl.: H01L 23/32 H01L 23/12

(22) Application date: 25.12.97

(30) Priority: 03.01.97 US 97 775981

(43) Date of application publication: 07.08.98

(84) Designated contracting states:

(71) Applicant: MOTOROLA INC

(72) Inventor: GREER STUART E  
CLEGG DAVID  
BURNETTE TERRY EDWARD

(74) Representative:

## (54) PACKAGING METHOD FOR INTEGRATED CIRCUIT

## (57) Abstract:

PROBLEM TO BE SOLVED: To realize a CPAC process which restrains the necessity for a number of devices and increase in cost, and attains a lower manufacturing cost, in order to secure connectability to a semiconductor device with respect to packaging of a semiconductor device having a solder bump structure attached thereto.

SOLUTION: Multiple coupling of solder bumps to various boards includes positioning of a semiconductor substrate having a solder bump structure which contacts a ceramic plate board, and positioning of a CPAC structure which contacts a PAC ball by a single flow step. A method therefor includes preparation of a semiconductor device 310, 312 having a first interconnection structure 314 to be connected with the surface and a board having a plurality of metal pads, positioning of a second interconnection structure 354 to be aligned with and in contact with the metal pads, positioning of the first interconnection structure 314 to be aligned with and in contact with the metal pads, simultaneous reflow of the first interconnection structure 314 and the second interconnection structure 354, and connection of the semiconductor device 310, 312 and the second interconnection structure 354 to the metal pads of the board.

COPYRIGHT: (C)1998,JPO

